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BEFORE THE UNITED STATES PATENT OFFICE  
AS INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

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LETTER AND AMENDMENTS  
UNDER ARTICLE 34

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I hereby certify that this correspondence is being forwarded via telefacsimile 703-305-3230, to the ISA/US on  
Nov. 5, 2003

By: 

Sir:

This letter and amendments are being submitted under Article 34 for the above identified international application. The claims are being amended for clarity. ~~No new~~ matter is being added.

Substitute sheets for those pages of the application which are being amended are enclosed herewith. The substitute sheets include pages 10 through 13 to replace pages 10 through 13 containing the claims.

The substitute claims differ from the claims originally on file as follows:

Original claims 1-3, 5-11, 13-21, 23, 25, 26, 29, and 30 have been amended.

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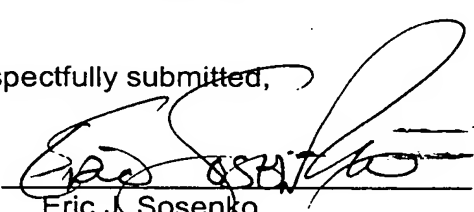
Original claims 22 and 24 have been cancelled. Substitute claims 1-21 maintain their original numbering. In view of the cancellation of claims 22 and 24, original claims 23, 25, 26, 27, 29, and 30 have been respectively renumbered as claims 22, 23, 24, 25, 26, and 27. Please note that the application was filed without a claim 28. This typographical error has been corrected by the renumbering of the claims.

Specifically, the claims have been amended such that the semiconductor multiplication and absorption layers are not characterized as "n-type" multiplication and absorption layers. Further, claim 1 has been amended to include the structural relationship "the semiconductor absorption layer is disposed between the semiconductor multiplication layer and the semiconductor layer with the p-type diffusion region"; claims 9, 17, and 19 have been amended to define a p-type diffusion layer with a smaller area than the semiconductor layer; and claim 19 has been further amended to include the words "wherein the photodiode has a low field region near the p-type semiconductor layer and a low capacitance."

In view of the above amendments it is respectfully submitted that the present form of the claims meets the criteria of the PCT and that a favorable International Preliminary Examination Report is now warranted with respect to all of the claims.

Respectfully submitted,

By:

  
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ocket No.: 10555-054

Dated: November 5, 2003

## CLAIMS

1. A planar avalanche photodiode comprising:  
a first n-type semiconductor layer defining a contact area;  
a second n-type semiconductor layer having a p-type diffusion region;  
an n-type semiconductor multiplication layer;  
an n-type semiconductor absorption layer; and  
a p-type contact layer;  
wherein the p-type diffusion region is disposed directly adjacent to the p-type contact layer.
2. The planar avalanche photodiode of claim 1 further comprising at least one grading layer disposed adjacent to the n-type semiconductor absorption layer.
3. The planar avalanche photodiode of claim 1 further comprising a p-type semiconductor charge control layer disposed adjacent to the n-type semiconductor multiplication layer.
4. The planar avalanche photodiode of claim 1 further comprising at least one n-type contact layer.
5. The planar avalanche photodiode of claim 1 wherein the first n-type semiconductor layer is InAlAs.
6. The planar avalanche photodiode of claim 1 wherein the second n-type semiconductor layer is InAlAs.
7. The planar avalanche photodiode of claim 1 wherein the n-type semiconductor multiplication layer is InAlAs.
8. The planar avalanche photodiode of claim 1 wherein the n-type semiconductor absorption layer is InGaAs.

9. A method of fabricating a planar avalanche photodiode comprising the following steps:

providing a first n-type semiconductor layer defining a contact area;  
 depositing a second n-type semiconductor layer;  
 depositing a n-type semiconductor multiplication layer;  
 depositing an n-type semiconductor absorption layer;  
 depositing a p-type contact layer; and  
 diffusing a p-type diffusion region directly adjacent to the p-type contact layer, thereby decreasing the capacitance of the planar avalanche photodiode.

10. The method of claim 9 further comprising the step of depositing at least one grading layer adjacent to the n-type semiconductor absorption layer.

11. The method of claim 9 further comprising the step of depositing a p-type semiconductor charge control layer adjacent to the n-type semiconductor multiplication layer.

12. The method of claim 9 further comprising the step of depositing at least one n-type contact layer.

13. The method of claim 9 wherein the first n-type semiconductor layer is InAlAs.

14. The method of claim 9 wherein the second n-type semiconductor layer is InAlAs.

15. The method of claim 9 wherein the n-type semiconductor multiplication layer is InAlAs.

16. The method of claim 9 wherein the n-type semiconductor absorption layer is InGaAs.

17. A planar avalanche photodiode including a first n-type semiconductor layer defining a contact area and a p-type contact area, the planar avalanche photodiode comprising:

- a second n-type semiconductor layer having a p-type diffusion region;
- an n-type semiconductor multiplication layer;
- an n-type semiconductor absorption layer; and

wherein the p-type diffusion region is disposed directly adjacent to the p-type contact layer.

18. The planar avalanche photodiode of claim 17 wherein the first n-type semiconductor layer is InAlAs, the second n-type semiconductor layer is InAlAs, the n-type semiconductor multiplication layer is InAlAs, and the n-type semiconductor absorption layer is InGaAs.

19. A planar avalanche photodiode comprising:

- a first n-type semiconductor layer defining a contact area;
- a p-type semiconductor layer;
- an n-type semiconductor multiplication layer;
- an n-type semiconductor absorption layer; and
- a p-type contact layer;

wherein the p-type semiconductor layer is disposed directly adjacent to the p-type contact layer.

20. The planar avalanche photodiode of claim 19 further comprising at least one grading layer disposed adjacent to the n-type semiconductor absorption layer.

21. The planar avalanche photodiode of claim 19 further comprising a p-type semiconductor charge control layer disposed adjacent to the n-type semiconductor multiplication layer.

22. The planar avalanche photodiode of claim 19 further comprising at least one n-type contact layer.

23. The planar avalanche photodiode of claim 19 wherein the first n-type semiconductor layer is InAlAs.

24. The planar avalanche photodiode of claim 19 wherein the second n-type semiconductor layer is InAlAs.

25. The planar avalanche photodiode of claim 19 wherein the n-type semiconductor multiplication layer is InAlAs.

26. The planar avalanche photodiode of claim 19 wherein the n-type semiconductor absorption layer is InGaAs.

27. The planar avalanche photodiode of claim 19 wherein the p-type semiconductor layer is InAlAs.

29. The planar avalanche photodiode of the claim 19 further comprising a passivated region, the passivated region comprising a portion of the p-type semiconductor layer and a portion of n-type semiconductor absorption layer.

30. The planar avalanche photodiode of claim 29 wherein the passivated region further comprises a portion of the first grading layer 18a and a portion of the n-type semiconductor multiplication layer 24.